

Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

- 1 (original): A phase adjusting circuit for generating a phase adjusting value based on the
5 phase difference of a target clock signal and an input signal, the phase adjusting circuit comprising:
a phase-frequency detector for generating a first control signal and a second control
signal by comparing the phase of the input signal with the phase of the target
clock signal;
10 a clock generator for generating a reference clock;
a counter connected to the phase-frequency detector and the counter for generating a
first counting value by counting the number of cycles of the reference clock
during the duration of the first control signal, and generating a second counting
value by counting the number of cycles of the reference clock during the
15 duration of the second control signal; and
a decision logic circuit connected to the counter for generating a third counting
value based on the first counting value and the second counting value,
calculating the sum of a plurality of the third counting values and comparing the
sum with a predetermined range for outputting the phase adjusting value as the
20 counting times are increased to equal to a predetermined counting times.
- 2 (original): The phase adjusting circuit of claim 1, wherein the first control signal is generated when the phase of the input signal leads the phase of the target clock signal.
- 25 3 (original): The phase adjusting circuit of claim 1, wherein the second control signal is generated when the phase of the input signal lags the phase of the target clock signal.

- 4 (original): The phase adjusting circuit of claim 1, wherein the predetermined range ranges from a positive number of a half of the predetermined counting times to a negative number having an absolute value of a half of the predetermined counting times.
- 5 5 (original): The phase adjusting circuit of claim 1, wherein the first counting value is a positive value, the second counting value is a negative value, and the third counting value is the sum of the first counting value and the second counting value.
- 10 6 (original): The phase adjusting circuit of claim 1, wherein the phase-frequency detector is further able to receive a protection signal to stop outputting the phase adjusting value for avoiding interference generated from an unstable input signal.
- 7 (currently amended): A clock signal adjusting circuit comprising:
15 a phase adjusting circuit for generating a phase adjusting value based on an input signal and a target clock signal, the phrase adjusting circuit comprising:
 a phase-frequency detector for generating a first control signal and a second control signal by comparing the phase of the input signal with the phase of the target clock signal;
 a clock generator for generating a second reference clock;
20 a counter connected to the phase-frequency detector and the clock generator for generating a first counting value by counting the number of cycles of the second reference clock during the duration of the first control signal, and generating a second counting value by counting the number of cycles of the second reference clock during the duration of the second control signal; and
25 a decision logic circuit connected to the counter for generating a third counting value based on the first counting value and the second counting value, calculating the sum of a plurality of the third counting values and comparing the sum with a predetermined range for outputting the phase

adjusting value as the counting times are increased to equal to a predetermined counting times; and

5 a frequency divider connected to the phase adjusting circuit for adjusting the target clock signal by dividing the frequency of a first reference clock based on the phase adjusting value.

8 (cancelled)

9 (currently amended): The clock signal adjusting circuit of ~~claim 8~~ claim 7, wherein the 10 first control signal is generated when the phase of the input signal leads the phase of the target clock signal.

10 (currently amended): The clock signal adjusting circuit of ~~claim 8~~ claim 7, wherein the second control signal is generated when the phase of the input signal lags the phase 15 of the target clock signal.

11 (currently amended): The clock signal adjusting circuit of ~~claim 8~~ claim 7, wherein the 20 predetermined range ranges from a positive number of a half of the predetermined counting times to a negative number having an absolute value of a half of the predetermined counting times.

12 (original): The clock signal adjusting circuit of claim 7, wherein the frequency divider comprises:

25 a counter for counting the cycle number of cycles of the first reference clock and resetting the cycle number after each predetermined number of cycles of the first reference clock;
a register for storing the phase adjusting value;
a comparator connected to the counter and the register for generating an enable

- signal when the cycle number of the first reference clock is equal to the phase adjusting value;
- a pulse generator connected to the comparator for generating an impulse when receiving the enable signal;
- 5 a flip-flop having a trigger input terminal connected to the pulse generator for outputting the target clock signal while receiving the impulse; and
- an inverter having an input terminal for receiving the target clock signal and inverting the target clock signal to feedback to the input of the flip-flop.
- 10 13 (original): The clock signal adjusting circuit of claim 7 being applied to an optical disc drive, the input signal being a wobble signal of an optical disc, the target clock signal being a corresponding wobble clock generated by the optical disc drive based on the wobble signal.
- 15 14 (currently amended): A method for adjusting clock signal comprising:
generating a phase adjusting value based on an input signal and a target clock signal;
- generating a first control signal and a second control signal by comparing the phase of the input signal with the phase of the target clock signal;
- generating a first counting value by counting the number of cycles of a second reference clock during the duration of the first control signal;
- generating a second counting value by counting the number of cycles of the second reference clock during the duration of the second control signal;
- generating a third counting value based on the first counting value and the second counting value;
- calculating the sum of a plurality of the third counting values and comparing the sum with a predetermined range for outputting the phase adjusting value as the counting times are increased to equal to a predetermined counting times; and
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adjusting the target clock signal by dividing the frequency of a first reference clock based on the phase adjusting value.

15 (cancelled)

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16 (currently amended): The method of ~~claim 15~~ claim 14, wherein the first control signal is generated when the phase of the input signal leads the phase of the target clock signal.

17 (currently amended): The method of ~~claim 15~~ claim 14, wherein the second control signal is generated when the phase of the input signal lags the phase of the target clock signal.

18 (currently amended): The method of ~~claim 15~~ claim 14, wherein the predetermined range ranges from a positive number of a half of the predetermined counting times to a negative number having an absolute value of a half of the predetermined counting times.

19 (original): The method of claim 14 further comprising:

counting the cycle number of cycles of the first reference clock and resetting the cycle number after each predetermined number of cycles of the first reference clock;

generating an enable signal when the cycle number of the first reference clock is equal to the phase adjusting value; generating an impulse when receiving the enable signal; outputting the target clock signal while receiving the impulse; and inverting the target clock signal to feedback to the input.

20 (original): The method of claim 14 being applied to an optical disc drive, the input signal being a wobble signal of an optical disc, the target clock signal being a

Appl. No. 10/709,022
Amdt. dated October 12, 2007
Reply to Office action of September 05, 2007

corresponding wobble clock generated by the optical disc drive based on the wobble signal.